IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Applicant: Ammar Derraa

Filed: Herewith

For: FIELD EMISSION DEVICE HAVING INSULATED COLUMN LINES AND METHOD OF MANUFACTURE

Box Patent Application
Assistant Commissioner for Patents
Washington, DC 20231

JC545 U.S. PTO 08/26/99

JC678 U.S. PTO 09/383331 08/26/99

TRANSMITTAL LETTER

Enclosed for filing are the following documents:

1. Application including 16 pages (specification 10 pages, claims 5 pages, and Abstract of the Disclosure 1 page);

2. Three sheets of informal drawings including Figs. 1-3;

3. Declaration;

4. Election Under 37C.F.R. §§ 3.71 and 3.73 and Power of Attorney;

5. Form PTO-1595 and Assignment; and

6. IDS, Form PTO-1449, and two references.

Please charge the $1,232 fee ($760 for the basic filing fee; $234 for three independent claim in excess of three; $198 for eleven claims in excess of twenty; and $40 for the assignment) to our deposit account no. 08-0219. Please also charge any additional fee or credit any overpayment in connection with this matter to our deposit account.

Respectfully submitted,

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August 26, 1999

Attorney Docket No. 100.718.422

EXPRESS MAIL LABEL NO. EL171836148US

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FIELD EMISSION DEVICE HAVING INSULATED COLUMN LINES AND METHOD OF MANUFACTURE

Field of the Invention

The present invention relates generally to flat panel displays and, more particularly, to field emission devices ("FEDs") and methods for manufacturing the same.

Background of the Invention

As is well known, FED technology operates on the principle of cathodoluminescent phosphors being excited by cold cathode field emission electrons. FIGURE 1 is a simplified illustration of a representative portion of a prior art FED device 10. In general, the FED device 10 comprises a cathode assembly 6 and an anode assembly 8 separated from each other by spacers 4.

The cathode assembly 6 is typically manufactured using conventional photolithographic processes to form successively defined features on a substrate or baseplate 12. In general, a conductive emitter electrode structure 14 is first formed on the substrate 12. Next, a resistive layer 15 is deposited over the conductive structure 14. A pattern of spaced-apart conical cold cathode emitter tips or micropoints 18 is then formed on the substrate, followed by a dielectric structure 20 and a conductive grid structure 22.

The substrate or baseplate 12 is typically formed of glass. The conductive structure 14 may be formed of a metal. The micropoints may be constructed of a number of materials such as, e.g., silicon or molybdenum.

The conductive structure 14 with the covering resistive layer 15 encircles the emitters 18 of a pixel group (described below). The portions of the conductive

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structure 14 shown in FIGURE 1 are thus electrically connected and form a column line, which is part of an addressable matrix as will be described below.

The resistive layer 15 comprising, e.g., amorphous silicon, covers the top and sides of the conductive structure 14. As shown, the outer sides of the base of each conical micropoint 18 are in contact with the resistive layer covering the conductive structure 14. The resistive layer 15 separates the conductive structure 14 from the micropoints 18 and helps prevent damage to the tips of the micropoint emitters 18.

After the micropoints 18 have been formed on the base plate 12, a dielectric layer is deposited over the micropoints 18 and the resistive layer 15. The dielectric layer, which is later formed into the dielectric structure 20, may comprise silicon dioxide or other materials. Next, a conductive layer is deposited over the dielectric layer. This conductive layer, which is later formed into the extraction grid structure 22, may be made from a variety of materials including chromium, molybdenum and doped polysilicon. Then, using a photolithography/etch process, the dielectric layer and the conductive layer are etched to form the dielectric and extraction structures 20, 22, respectively, which surround, but are spaced away from the micropoints 18 as shown in FIGURE 1.

The extraction structure 22 forms a low potential anode that is used to extract electrons from the micropoints 18. The extraction structure has a grid construction comprising multiple row lines that are orthogonal to the column lines formed by the conductive structure 14. The row and column lines are part of the addressable matrix as described below.

The anode assembly 8 usually has a transparent (e.g., glass) substrate 24 and a transparent conductive layer 26 formed over the substrate 24 (on the side facing cathode assembly 6). A black matrix grill 25 is formed over the conductive layer 26 to define pixel regions 28, in which a cathodoluminescent coating is deposited.

The anode assembly 8 is typically manufactured using conventional

photolithography processes to form successively defined features on the lower (as shown in FIGURE 1) surface of the transparent substrate 24, starting with transparent conductive layer 26. The next features usually formed are the spacers 4, which project downwardly (e.g., about 150 microns) from conductive layer 26. The black matrix grill 25 is then formed defining the pixel regions 28, in which phosphor material is deposited.

When assembled, the anode assembly 8 is positioned a predetermined distance from the cathode assembly 6 (and from micropoint emitters 18) by the spacers 4.

A power supply 30 is electrically coupled to the conductive layer 26 of the anode assembly 8 and to the conductive layer 14 (at the base of the micropoint emitters 18) and the conductive grid structure 22 of the cathode assembly 6. A vacuum in the space between cathode 6 and anode 8 facilitates travel of electrons emitted from the micropoints 18 towards the pixel regions 28 to impact the pixel regions. The emitted electrons strike the cathodoluminescent coating in the pixel regions 28, which emits light to form a video image on a display screen formed by the anode 8.

The visible display of the FED 10 is normally arranged as a matrix of pixels, one of which (32) is shown in FIGURE 1. Each pixel in the display is typically associated with a group of micropoint emitters, with all emitters in a group being dedicated to controlling the brightness of their associated pixel. For example, FIGURE 1 shows a single pixel 32, with the pixel being associated with emitters 18. For convenience of illustration, FIGURE 1 shows a line of four emitters as being associated with the single pixel 32. Pixel 32 could be a single pixel of a black and white display or a single red, green, or blue dot associated with a single pixel of a color display.

The row lines of the extraction structure 22 and the column lines of the

emitter electrode structure 14 form an addressing matrix for selectively activating pixels. Normally, the row and column lines are arranged so that the emitters associated with one pixel can be controlled independently of all other emitters in the display and so that all emitters associated with a single pixel are controlled in unison. In operation, a row signal activates a single conductive row line within the extraction grid 22, while a column signal activates a conductive column line within the emitter base electrode 14. At the intersection of an activated column and an activated row, a grid-to-emitter voltage differential sufficient to induce field emission will exist, causing illumination of a respective pixel.

Conventional photolithography processes are typically used to fabricate the various structures (e.g., the conductive strips 14) of the FED 10.

It has been found in prior art FEDs that the addressing column line structure 14 sometimes electrically shorts to the row line structure 22. Such electrical shorting degrades the quality of the display and can even make the FED inoperative. The shorting is believed to result from manufacturing flaws in FEDs. For example, intrinsic defects in the dielectric structure 20 may effectively form conductive paths between the column addressing line and the grid. In addition, variations in the substrate and grid surfaces that cause the surfaces to be closer than intended may also cause shorting. A need therefore exists for an improved FED construction that significantly reduces the possibility of electrical shorting between column and row lines.

Brief Summary of the Invention

The present invention is directed to an FED that has a cathode assembly containing an improved addressing column line structure. The addressing column line structure includes a conductive structure formed on a substrate. A resistive layer is formed over the conductive structure, and an insulator layer is formed partly over the resistive layer. Electrical contact between the base of the emitter tips and the addressing column line is achieved through lateral sides of the conductive structure not covered by the insulator layer. The insulator layer helps reduce the possibility of electrical shorts between the column line and the row line structure of the cathode assembly. The insulator layer on top of the addressing column line will allow the use of a thinner subsequent dielectric layer. This thinner dielectric layer, which supports the grid, will provide a lower RC time constant and help achieve better video rate operation. The thinner dielectric layer also will result in smaller grid openings above the tips. This will provide for better beam spots, and, therefore, better image resolution. The thinner dielectric layer will require less applied voltage to extract electrons from the emitter tips, resulting in lower power consumption for the FED.

These and other advantages of the present invention will become readily apparent from the following detailed description wherein embodiments of the invention are shown and described by way of illustration of the best mode of the invention. As will be realized, the invention is capable of other and different embodiments, and its several details may be capable of modifications in various respects, all without departing from the invention. Accordingly, the drawings and description are to be regarded as illustrative in nature and not in a restrictive or limiting sense with the scope of the application being indicated in the claims.

Brief Description of the Drawings

For a fuller understanding of the nature and objects of the present invention, reference should be made to the following detailed description taken in connection with the accompanying drawings wherein:

FIGURE 1 is a cross-section view of a portion of an exemplary prior art FED;

FIGURE 2 is an enlarged cross-section view of a part of an FED in accordance with the invention which illustrates a portion of an insulated addressing column line and also the lateral contact between the base of the emitter tips and the addressing column line; and

FIGURE 3 is perspective view of a portion of the FED partly broken away to illustrate the inventive addressing column line structure in greater detail.

Detailed Description of the Preferred Embodiments

The present invention is directed to an improved FED, in which column addressing lines are insulated to reduce the possibility of shorting and to provide other benefits. FIGURES 2 and 3 show a small portion of the cathode assembly of an FED 100 illustrating the inventive column addressing line structure 102.

The inventive column line structure 102 (a small portion of which is shown) is preferably formed on a substrate or baseplate 104 of the cathode assembly. The column line structure 102 comprises a conductive layer 106, a resistive layer 108, and an insulator layer 110.

The conductive layer 106 is preferably formed like the layer 14 of the FED 10 of FIGURE 1. It may comprise a variety of conductive materials including metals. For example, the conductive layer 106 may comprise an aluminum layer having a thickness of about 1000 Å.

The resistive layer 108 is preferably similar to the resistive layer 15 in FIGURE 1 in that it covers the top and sides (as shown in the drawings) of the conductive layer 106. The resistive layer 108 may comprise various materials including silicon. For instance, the resistive layer 108 may be boron doped silicon having a thickness also of about 1000 Å.

The insulator layer 110 has higher resistivity than the resistive layer 108. It is preferably formed to cover just the top of the resistive layer. If the insulator layer 110 also covered an entire side of the resistor layer 108, then the insulator layer 110 might interfere with electrical communication between the conductive layer 106 and the adjacent emitter 112. Therefore, as shown in FIGURES 2 and 3, insulator layer 110 preferably covers the top and not the sides of the resistive layer 108. However, in an alternative embodiment, the insulator layer 110 could also cover selected portions of the sides of the resistive layer 108.

The insulator layer 110 may be made of various insulative materials including, e.g., silicon dioxide or silicon nitride. The insulator layer 110 may have a thickness of about 1000 Å. The combination of resistive layer 108 and insulator layer 110 together preferably introduce a substantial amount of resistivity, preferably, in excess of 1 megaohm between conductive layer 106 and the grid 116.

The insulator layer 110 is to assist in reducing shorts between the addressing column line and the row lines on the grid. The dielectric layer 114 is used to support the grid 116 above the emitter tips 112. It is to be understood that the insulator layer 110 and the dielectric layer 114 may be made of the same or different material and still be within the scope of the present invention. Regardless of whether the same or different materials are used, as will be discussed below, the insulator layer 110 and the dielectric layer 114 are preferably separately formed. The insulator layer 110 reduces the possibility of shorting between the addressing column line structure and the row line structure, which as previously discussed may result from, e.g., intrinsic defects in the dielectric structure or unintended variations in spacing between the substrate and grid surfaces.

It should be recognized that a variety of alternative materials of different thicknesses may be used for the conductive layer 106, the resistive layer 108, and the insulative layer 110.

The improved addressing line structure 102 is preferably fabricated as follows. First, the conductive layer 106 is formed on the baseplate 104 using conventional photolithography techniques. Specifically, a layer of material from which the structure 106 is to be formed is first deposited on the baseplate 104 using conventional deposition techniques. Then, using conventional a photolithography/etch/strip sequence, the conductive layer structure 106 is formed.

Thereafter, the resistive and insulative layers 108, 110 are formed. First, a layer of material from which the resistive layer 108 is formed is deposited over the pattern of conductive strips 106. Then, a layer of material from which the insulator layer 110 is formed is deposited over the layer of resistive material. Next, using a conventional photolithography/etch/strip sequence, the resistive layer 108 and insulator layer 110 are formed on the conductive layer structure 106.

To complete fabrication of the cathode assembly, the micropoint emitters 112, the dielectric structure 114, and the conductive grid structure 116 are then formed preferably using conventional photolithography techniques. The micropoint emitters 112 are preferably formed such that the addressing line structure 102 is disposed around (and in contact with) adjacent micropoint emitters 112 associated with a given pixel. The insulating layer deposited over the resistive layer 108, which covers the conductive structure 106, does not affect the electrical relationship between the conductive structure 106 and the adjacent emitters 112 because the sides of the addressing line structure 102 in contact with the emitters are not insulated.

The cathode assembly formed with the inventive column addressing line structure can be assembled with a conventional anode assembly like that shown in FIGURE 1 to form an FED.

Adding the insulating layer 110 to the addressing lines requires one additional deposition step in FED fabrication, namely the step of depositing the insulating layer 110 on top of the resistor layer 108. However, no extra photolithography sequences are required for forming the insulating structure 110 because the insulator and resistor layers 110, 108 are etched from a single mask pattern. This is possible because when viewed from the top, in the preferred embodiment of the addressing line, (as shown in FIGURE 2) the outer edges of the insulating structure 110 and the underlying resistive layer structure 108 are

substantially aligned, i.e., the insulator structure 110 substantially exactly overlies the resistor layer 108. Therefore, no extra photolithography (or masking) steps are needed, which are well known to be costly, complex and time consuming.

Many variations of the above-described preferred embodiments are possible. For example, one alternative embodiment might include more layers than the above-described combination of an insulator layer 110 and a resistive layer 108. For example, multiple resistive layers, could be layered on top of one another to form a suitably high series resistance.

It has been found that by insulating column addressing lines in accordance with the invention, there is a significantly reduced possibility of shorting between column and row lines when the FED is in use.

The insulated column line structure also provides other advantages. For instance, addition of the insulative layer 110 increases the distance between the conductive layer 106 and the grid structure 116. This improves the FED's refresh rate by decreasing the associated RC constant. 'R' is the resistance of the conductive lines (both grid and column), and 'C' is the capacitance between a column line and the grid layer. C is proportional to A/d (where 'A' is a cross sectional area and 'd' is the distance between the plates). By increasing d, C is reduced, which thereby reduces the RC constant. The reduced RC time constant will assist in achieving a better video rate operation of the display.

Other benefits of the invention include an ability to use thinner dielectric layers 114, which allows smaller cavity openings around the emitter tip to be constructed. This consequently reduces the beam spot and improves display images.

Having described embodiments of the present invention, it should be apparent that modifications can be made without departing from the scope of the present invention.

Claims

1. A method of making a cathode assembly of an FED, comprising:

providing a substrate;

forming an emitter electrode structure on the substrate;

forming a resistive layer over the emitter electrode structure;

forming an insulative layer on a portion of the resistive layer;

forming at least one micropoint emitter in contact with the resistive layer;

forming a conductive grid structure spaced from the at least one micropoint; and

forming a dielectric structure spaced from the at least one micropoint and between the insulative layer and the grid structure.

2. The method of Claim 1 wherein said emitter electrode structure comprises metal.

3. The method of Claim 1 wherein said emitter electrode structure comprises aluminum.

4. The method of Claim 1 wherein said resistive layer comprises silicon.

5. The method of Claim 1 wherein said insulative layer comprises silicon oxide.

6. The method of Claim 1 wherein said insulative layer comprises silicon nitride.

7. The method of Claim 1 wherein said insulative layer comprises a strip having a thickness of about 1000 Å.

8. The method of Claim 1 wherein said structure comprises glass.

9. The method of Claim 1 wherein forming said conductive grid structure and said dielectric structure comprise:

depositing a dielectric layer over the insulative layer and said at least one micropoint emitter;

depositing a conductive layer over the dielectric layer; and

selectively etching openings through the conductive and dielectric layers to expose the at least one micropoint emitter, with walls defining the openings being spaced away from the at least one micropoint emitter.

10. A column line structure for use in a cathode assembly of an FED, comprising:

a conductive structure;

a resistive layer formed on said conductive structure; and

an insulative layer formed partly over said resistive layer.

11. The column line structure of Claim 9 wherein said conductive structure comprises metal.

12. The column line structure of Claim 9 wherein said conductive structure comprises aluminum.

13. The column line structure of Claim 9 wherein said resistive layer comprises silicon.

14. The column line structure of Claim 9 wherein said insulative layer comprises silicon oxide.

15. The column line structure of Claim 9 wherein said insulative layer comprises silicon nitride.

16. The column line structure of Claim 9 wherein said insulative layer comprises a strip having a thickness of about 1000 Å.

17. In a method of making a field emission device, a method of making a column line structure for an addressing matrix, comprising:

forming a conductive structure;

forming a resistive layer on said conductive structure; and

forming an insulative layer partly covering said resistive layer.

18. The method of Claim 17 wherein said conductive structure comprises metal.

19. The method of Claim 17 wherein said conductive structure comprises aluminum.

20. The method of Claim 17 wherein said resistive layer comprises silicon.

21. The method of Claim 17 wherein said insulative layer comprises silicon oxide.

22. The method of Claim 17 wherein said insulative layer comprises silicon nitride.

23. The method of Claim 17 wherein said insulative layer comprises a strip having a thickness of about 1000 Å.

24. A method of making an FED, comprising: making a cathode assembly, making an anode assembly, and assembling said cathode and anode assemblies, wherein said step of making a cathode assembly includes forming an insulation layer on column lines forming part of an addressing matrix to reduce the possibility of shorting between the column lines and a conductive grid structure of the FED.

25. An FED, comprising a cathode assembly and an anode assembly assembled with said cathode assembly, wherein said cathode assembly includes an addressing matrix comprising multiple row lines and column lines, said column lines having an insulation layer thereon to inhibit shorting with the row lines.

26. A method of making an FED, comprising:

making a cathode assembly, making an anode assembly, and assembling the cathode and anode assemblies,

wherein said step of making a cathode assembly comprises

providing a substrate;

forming an emitter electrode structure on the substrate;

forming a resistive layer over the emitter electrode structure;

forming an insulative layer on a portion of the resistive layer;

forming at least one micropoint emitter in contact with the resistive layer;

forming a conductive grid structure spaced from the at least one micropoint; and

forming a dielectric structure spaced from the at least one micropoint and between the insulative layer and the grid structure.

27. The method of Claim 26 wherein said emitter electrode structure comprises metal strips.

28. The method of Claim 26 wherein said emitter electrode structure comprises aluminum strips.

29. The method of Claim 28 wherein said aluminum strips have a thickness of about 1000 Å.

30. The method of Claim 26 wherein said insulative layer comprises silicon oxide.

31. The method of Claim 26 wherein said insulative layer comprises silicon nitride.

FIELD EMISSION DEVICE HAVING INSULATED COLUMN LINES AND METHOD OF MANUFACTURE

Abstract of the Disclosure

An FED and a method of manufacture are provided. The FED includes a cathode assembly containing an improved column line structure. The column line structure includes a conductive structure formed on a substrate. A resistive layer is formed on the conductive structure, and an insulator layer is formed partly over the resistive layer. The contact between the base of the emitter tips and the addressing column line is achieved through a lateral side that is not covered by the insulator layer. The insulator layer helps reduce the possibility of electrical shorting between the addressing column line and the row line structure of the cathode assembly. The insulator layer on top of the addressing column line will allow the use of a thinner subsequent dielectric layer. This thinner dielectric layer, which supports the grid, will provide a lower RC time constant and help achieve better video rate operation. The thinner dielectric layer also will result in smaller grid openings above the tips. This will provide for better beam spots, and, therefore, better image resolution. The thinner dielectric layer will require less applied voltage to extract electrons from the tips, resulting in lower power consumption for the FED.

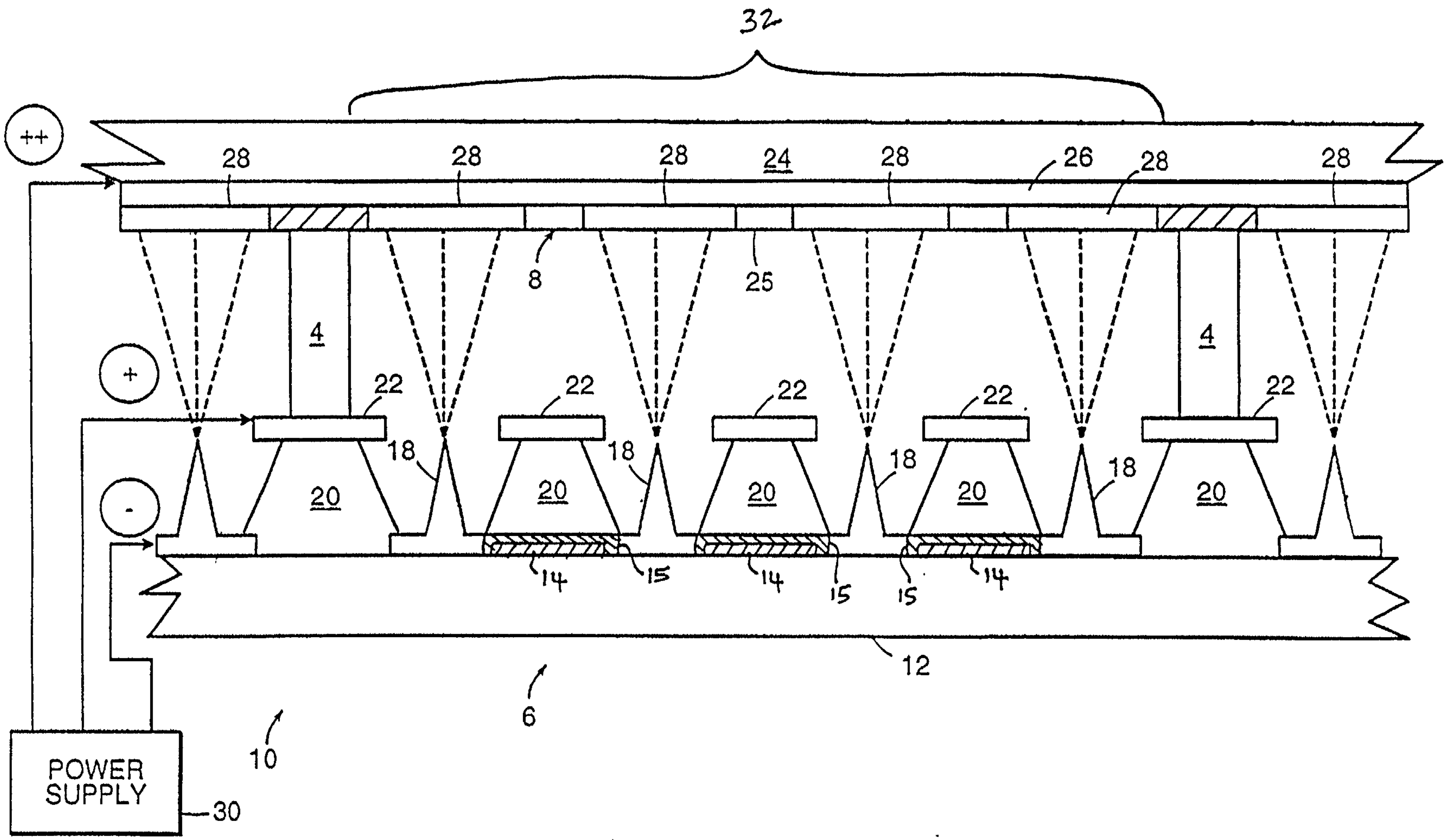

FIG. 1
PRIOR ART

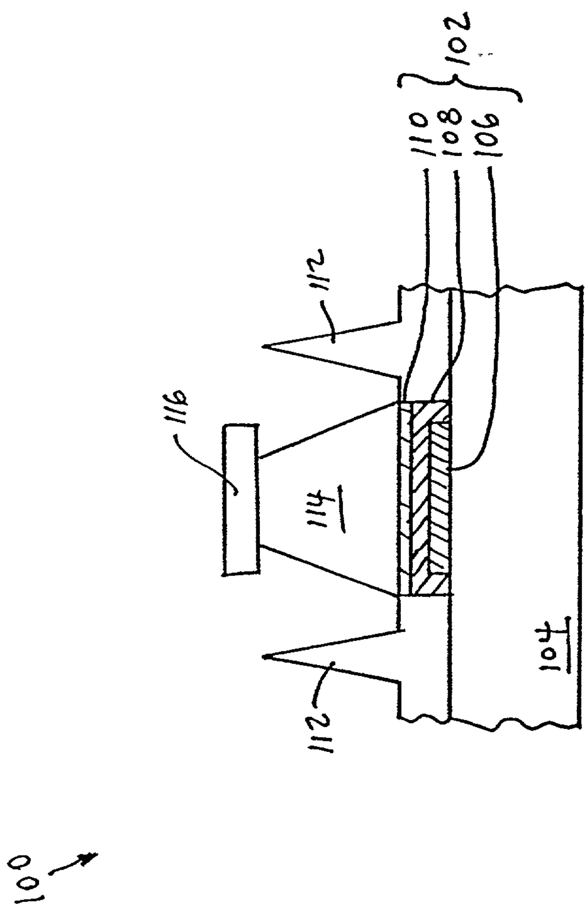

FIG. 2

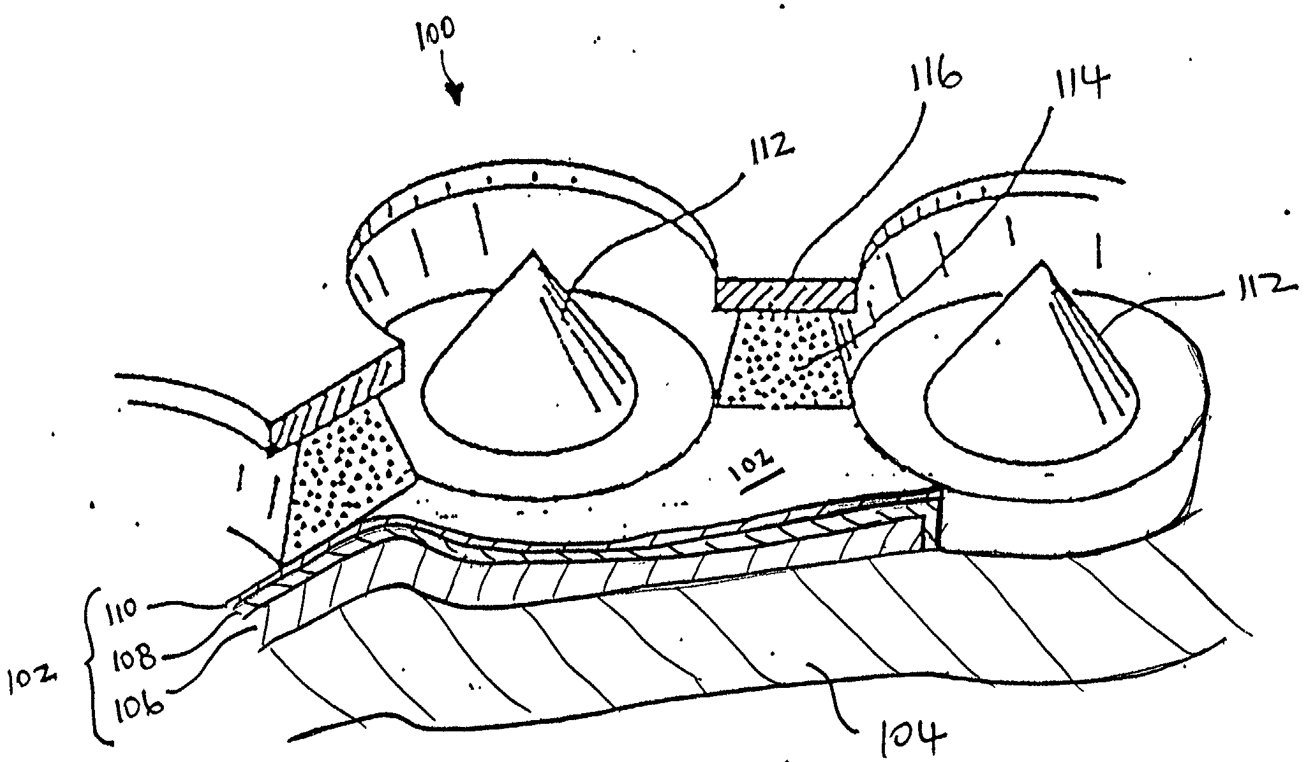

FIG. 3

DECLARATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled **FIELD EMISSION DEVICE HAVING INSULATED COLUMN LINES AND METHOD OF MANUFACTURE**, the specification of which is

__X__ is attached hereto.

_____ was filed on ________________, as Application Serial No. ________.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

I acknowledge the duty to disclose information which is material to patentability of the subjected matter claimed in this application as "materiality" is defined in Title 37 of the Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

PRIOR FOREIGN/PCT APPLICATION(S) AND ANY PRIORITY CLAIMS UNDER 35 U.S.C. §119(a)-(d) or 365(b):

COUNTRY (if PCT indicate PCT)	APPLICATION NUMBER	DATE OF FILING	PRIORITY CLAIMED UNDER 35 U.S.C. §119(a)-(b) or 365(b) (YES/NO)

I hereby claim the benefit under 35 U.S.C. §119(e) of any United States provisional patent application(s) listed below:

APPLICATION NUMBER	DATE OF FILING	STATUS: (PENDING OR ABANDONED)

EXPRESS MAIL LABEL NO. EL171836148US

DATE OF DEPOSIT AUGUST 26 1999

I hereby claim the benefit under Title 35, United States Code, § 120 or 365(c) of any United States application(s) or PCT international application(s) designating the United States of America that is/are listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, § 112. I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56 which occurred between the filing date of the prior applications and the national or PCT international filing date of this application:

PRIOR U.S. APPLICATION OR PCT INTERNATIONAL APPLICATION(S) DESIGNATING THE U.S. FOR BENEFIT UNDER 35 U.S.C. § 120 or 365(c):

APPLICATION NUMBER	DATE OF FILING (day, month, year)	STATUS: (PATENTED, PENDING OR ABANDONED)

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Title 18 of the United States Code, § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of first or sole inventor: Ammar Derraa

Inventor's Signature:

Date: Aug 24th, 1999

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Citizenship: Algeria - Canada

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Ammar Derraa

Filed: Herewith

For: **FIELD EMISSION DEVICE HAVING INSULATED COLUMN LINES AND METHOD OF MANUFACTURE**

Attorney Docket No.: MIC-80/98-0716

ELECTION UNDER 37 C.F.R. §§ 3.71 AND 3.73 AND POWER OF ATTORNEY

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

The undersigned, being Assignee of the entire interest in the above-identified application by virtue of an Assignment recorded in the United States Patent and Trademark Office as set forth below or filed herewith, hereby elects, under 37 C.F.R. § 3.71, to prosecute the application to the exclusion of the inventor(s).

The Assignee hereby revokes any previous Power of Attorney and appoints: James B. Lampert, Reg. No. 24,564; Michael J. Bevilacqua, Reg. No. 31,091; Wayne M. Kennard, Reg. No. 30,271; Donald R. Steinberg, Reg. No. 37,241; Hollie L. Baker, Reg. No. 31,321; Wayne A. Keown, Reg. No. 33,923; Michael A. Diener, Reg. No. 37,122; Richard A. Goldenberg, Reg. No. 38,895; Peter M. Dichiara, Reg. No. 38,005; Keum J. Park, Reg. No. 42,059; Jason A. Reyes, Reg. No. 41,513; Ann-Louise Kerner, Reg. No. 33,523; Gretchen A. Rice, Reg. No. 37,429; Colleen Superko, Reg. No. 39,850; Rajesh Vallabh, Reg. No. 35,761; Henry N. Wixon, Reg. No. 32,073; Michael L. Lynch, Reg. No. 30,871; and, Lia M. Pappas, Reg. No. 34,095 as its attorney or agent, with full power of substitution and revocation, to prosecute the application, to make alterations and amendments therein, to transact all business in the Patent and Trademark Office in connection therewith, to receive any Letters Patent, and for one year after issuance of such Letters Patent to file any request for a certificate of correction that may be deemed appropriate.

Pursuant to 37 C.F.R. § 3.73, the undersigned duly authorized designee of Assignee certifies that the evidentiary documents have been reviewed, specifically the Assignment to MICRON TECHNOLOGY, INC. referenced below, and certifies that to the best of my knowledge and belief, title remains in the name of the Assignee.

Assignment

X Filed concurrently herewith for recording, a copy of which is attached hereto.

____ Previously recorded on ____________, at Reel: ________ Frame: ________.

Please direct all communications as follows:

Rajesh Vallabh
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ASSIGNEE: MICRON TECHNOLOGY, INC.

Date: 8-24-99

By: ____________________
Michael L. Lynch, Reg. No. 30,871
Chief Patent Counsel

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DATE OF DEPOSIT August 26, 1999

4. Warrant that I have not knowingly conveyed to others any right in said inventions, discoveries, applications, or patents, or any license to use the same, or to make, use, or sell anything embodying or utilizing any of said inventions or discoveries; and that I have good right to assign the same to ASSIGNEE without encumbrance;

5. Bind my heirs, legal representatives, and assigns, as well as myself, to do, upon ASSIGNEE's request and at ASSIGNEE's expense, but without additional consideration to me or them, all acts reasonably serving to assure that said inventions and discoveries, said patent applications, and said Letters Patents shall be held and enjoyed by ASSIGNEE as fully and entirely as the same could have been held and enjoyed by me, our heirs, legal representatives, and assigns if this Assignment had not been made; and particularly to execute and deliver to ASSIGNEE all lawful application documents including petitions, specifications, and oaths, and all assignments, disclaimers, and lawful affidavits in form and substance as may be requested by ASSIGNEE; and to communicate to ASSIGNEE all facts known to me relating to said inventions and discoveries or the history thereof, and to testify as to the same in any court or proceeding; and to furnish ASSIGNEE any and all documents, photographs, models, samples, and other physical exhibits in my control or in the control of my heirs, legal representatives, or assigns which may be useful for establishing the facts of my conceptions, disclosures, and reduction to practice of said inventions and discoveries.

IN TESTIMONY WHEREOF, I have hereunto set my hand and seal.

DATE: Aug. 24, 1999

Ammar Derraa

WITNESSED BY:

Trish Honan-Haider

Name

My Commission Expires 3-26-03

Boise ID 83716

Address

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